

Patent Abstracts of Japan

PUBLICATION NUMBER : 10074887
PUBLICATION DATE : 17-03-98

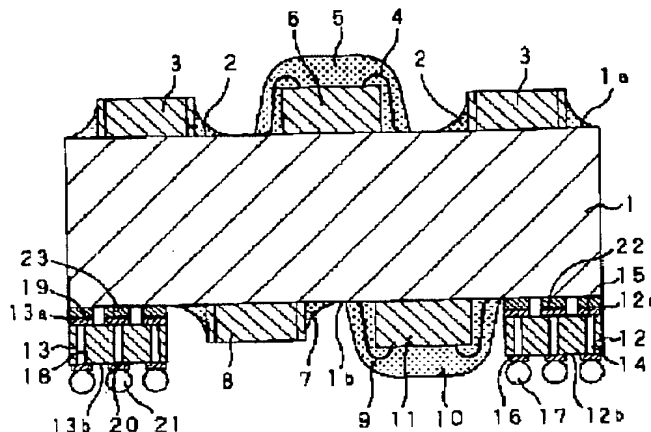
APPLICATION DATE : 30-08-96
APPLICATION NUMBER : 08231049

APPLICANT : SONY CORP;

INVENTOR : ITOU MUTSUSADA;

INT.CL. : H01L 25/04 H01L 25/18 H01L 23/32 //
H01L 23/12

TITLE : ELECTRONIC PART AND ITS
MANUFACTURE



ABSTRACT : PROBLEM TO BE SOLVED: To enable mounting of a chip part on a solder ball formation side for improving its mounting density.

SOLUTION: Chip parts 3, 6, 8 and 11 are mounted on opposing major surfaces 1a and 1b of a substrate 1 respectively, and spacers 12 and 13 which are higher in level than the mounted chip parts 8 and 11 are mounted also on the major surface 1b. The spacers 12 and 13 are arranged so that one major surfaces 12a and 13a of the spacers facing the substrate are conducted with major surfaces 12b and 13b thereof opposed thereto, solder balls 17 and 21 are placed on the spacers 12 and 13 to be connected with the chip parts 3, 6, 8, and 11 through the spacer 12 and 13, and function as terminals for interconnection with the external devices.

COPYRIGHT: (C) JPO

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-074887

(43)Date of publication of application : 17.03.1998

(51)Int.Cl.

H01L 25/04

H01L 25/18

H01L 23/32

// H01L 23/12

(21)Application number : 08-231049

(71)Applicant : SONY CORP

(22)Date of filing : 30.08.1996

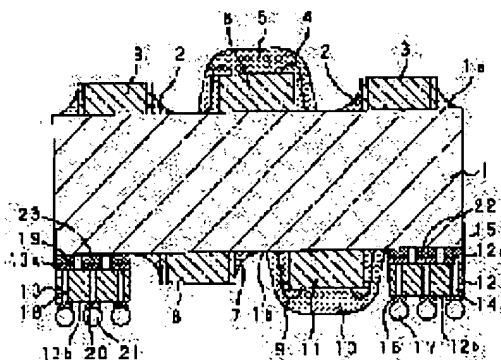
(72)Inventor : YOSHIMURA TAKAHISA
ITOU MUTSUSADA

(54) ELECTRONIC PART AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To enable mounting of a chip part on a solder ball formation side for improving its mounting density.

SOLUTION: Chip parts 3, 6, 8 and 11 are mounted on opposing major surfaces 1a and 1b of a substrate 1 respectively, and spacers 12 and 13 which are higher in level than the mounted chip parts 8 and 11 are mounted also on the major surface 1b. The spacers 12 and 13 are arranged so that one major surfaces 12a and 13a of the spacers facing the substrate are conducted with major surfaces 12b and 13b thereof opposed thereto, solder balls 17 and 21 are placed on the spacers 12 and 13 to be connected with the chip parts 3, 6, 8, and 11 through the spacer 12 and 13, and function as terminals for interconnection with the external devices.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's

Searching PAJ

decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2000 Japan Patent Office